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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,684	01/29/2004	Ashraf W. Lotfi	ENP-004	7088

25962 7590 02/10/2006

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EXAMINER	
ERDEM, FAZLI	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/767,684	LOTFI ET AL.	
	Examiner	Art Unit	
	Fazli Erdem	2826	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7,15-22,24,25,37 and 38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-22,24,25 and 38* is/are allowed.

6)☒ Claim(s) *1,3,4,6,7 and 37* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/22/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 15-22, 24, 25 and 38 allowed.

1. Claims 5 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, 4 and 37 rejected under 35 U.S.C. 103(a) as being unpatentable over Mihnea et al. (6,384,447) in view of Gardner et al. (5,710,054) further in view of Sicard et al.

Regarding Claims 1, 3, 4 and 37, Mihnea et al. disclose a source/drain regions 112 and 115 including a lightly doped region 133 and heavily doped region 136 adjacent to each other, an oppositely doped well region 128 under and within the channel region 162, , doped region 139 located between the heavily doped region 136 and oppositely doped well region 128 having a doping concentration profile less than a doping concentration profile of the heavily doped region. Mihnea et al. fail to disclose the required adjacent structure between lightly and heavily doped regions and the required buried layer. However, Gardner et al. disclose a method of forming a shallow junction by

diffusion from a silicon-based spacer where in Fig. 6F, lightly and heavily doped regions N- and N+ are situated in a required adjacent manner. Furthermore, Sicard et al. disclose a semiconductor device and method for protecting such device from a reversed drain voltage where in Fig. 3, N type buried layer 24 is located under the P type doped region 31.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required adjacent structure of lightly and heavily doped regions and oppositely doped buried layer under the doped region in Mihnea et al. as taught by Gardner et al. and Sicard et al., respectively, in order to have semiconductor device with increased performance and reliability.

4. Claims 6 and 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Mihnea et al. (6,384,447) in view of Sicard et al. (6,413,806) further in view of Cai et al. (2004/0227190) further in view of Gardner et al. (5,710,054)

Regarding Claims 6,7, 15-21, 24 and 25, Mihnea et al. disclose a source/drain regions 112 and 115 including a lightly doped region 133 and heavily doped region 136 adjacent to each other, an oppositely doped well region 128 under and within the channel region 162, , doped region 139 located between the heavily doped region 136 and oppositely doped well region 128 having a doping concentration profile less than a doping concentration profile of the heavily doped region. Mihnea et al. fail to disclose the required buried layer, LDMOS, sidewall/spacers and the required adjacent structure between lightly and heavily doped regions. However, Sicard et al. disclose a

semiconductor device and method for protecting such device from a reverses drain voltage where in Fig. 3, oppositely N doped buried layer 24 is located under P-doped region 31. Furthermore, Cai et al. disclose an ESD protection for semiconductor products where in Fig. 1, LDMOS structure has sidewall spacers 44. Finally, Gardner et al. disclose a method of forming a shallow junction by diffusion from a silicon-based spacer where in Fig. 6F, lightly and heavily doped regions N- and N+ are situated in a required adjacent manner.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required buried layer, LDMOS, sidewall spacers and the required adjacent structure of lightly and heavily doped regions in Mihnea et al. as taught by Cai. et al. and Gardner et al. in order to have semiconductor device with increased performance and reliability.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (571) 272-1914. The examiner can normally be reached on M - F 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

FE
February 5, 2006